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(19) United States

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Yamamoto et al. (43) Pub. Date: Jan. 22, 2004

(54) SIGNAL RECEIVING APPARATUS AND GAIN CONTROL METHOD USING ANALOG CONTROL AGC AND STEP CONTROL AGC

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Publication Classification

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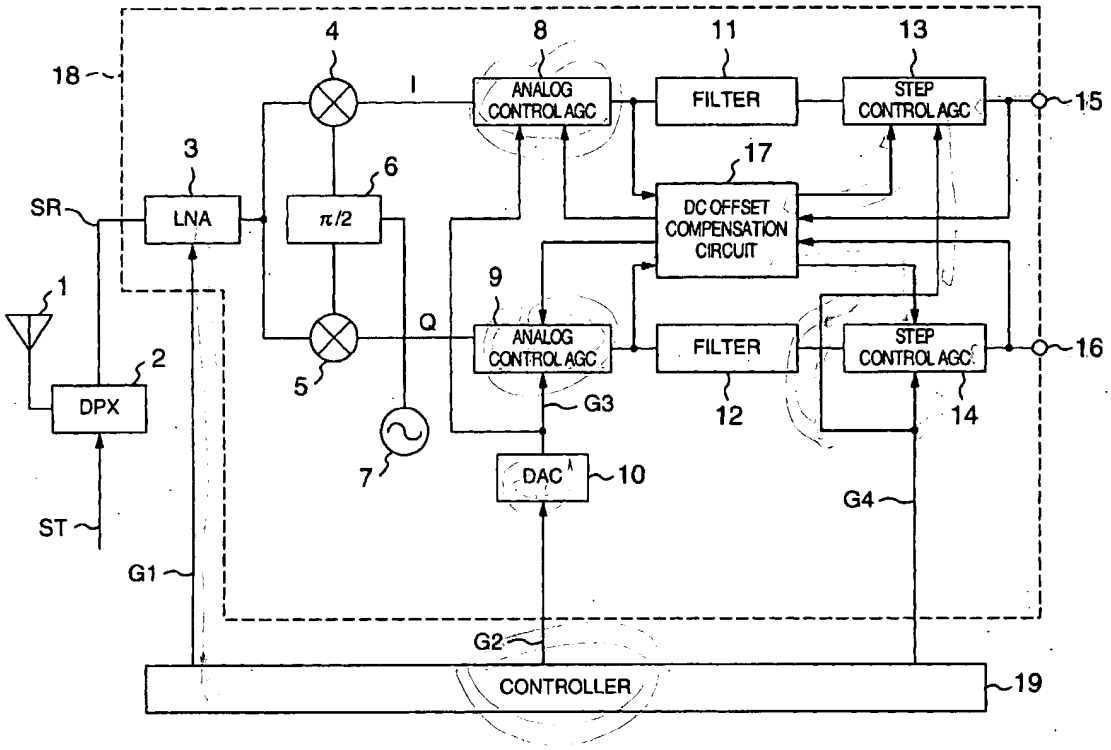
(52) U.S. Cl. 455/307; 455/280

(57) ABSTRACT

A signal receiving apparatus comprises an analog control AGC having a continuously varying gain and a step control AGC having a gain switched in steps, one of which is used to control the gain of a baseband signal, and the other of which is used to control the gain of the gain controlled signal.



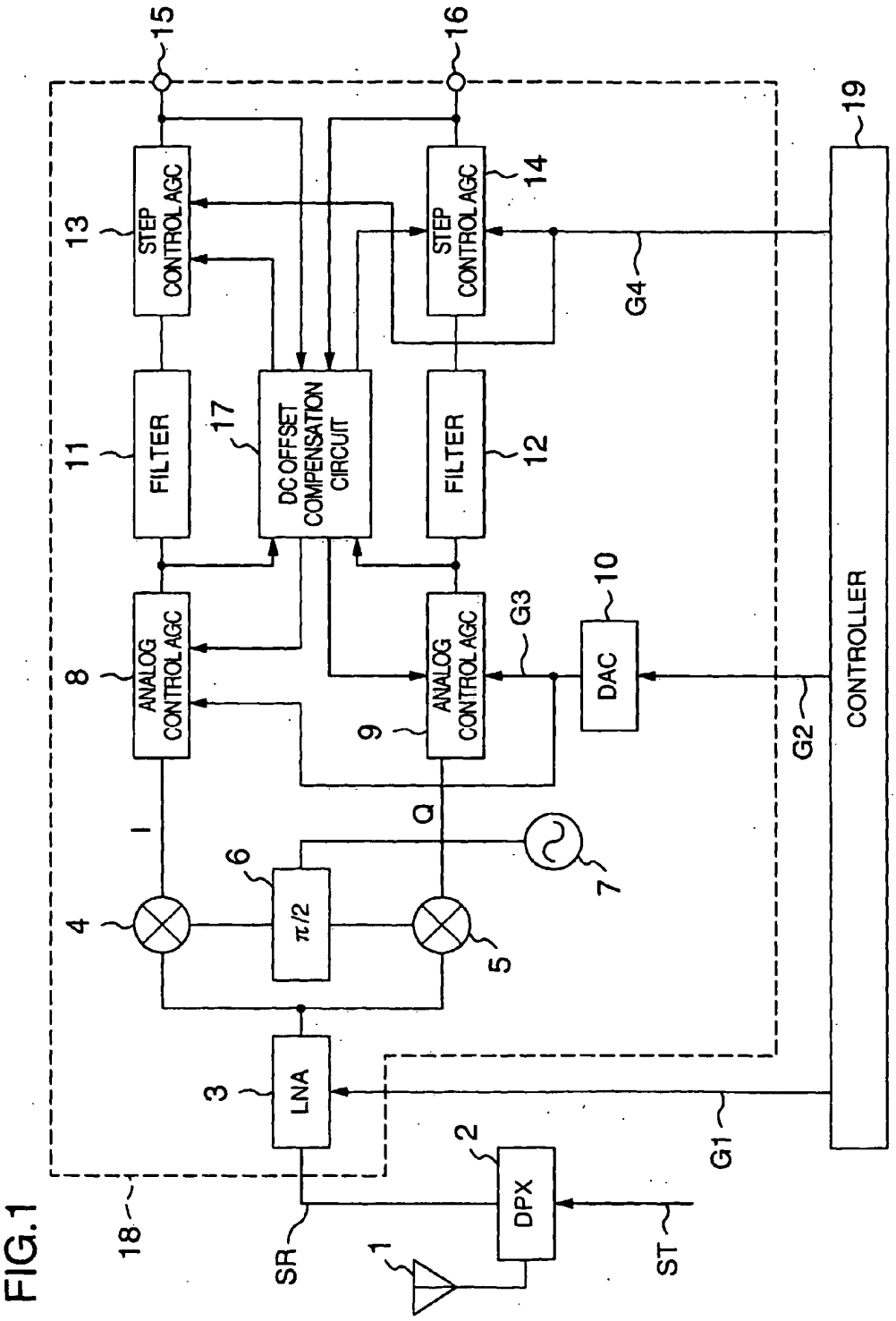

15
16
19
13
STEP CONTROL AGC
14
STEP CONTROL AGC
G4
11
FILTER
17
DC OFFSET COMPENSATION CIRCUIT
FILTER
12
8
ANALOG CONTROL AGC
9
ANALOG CONTROL AGC
G3
10
DAC
CONTROLLER
G2
I
Q
6
π/2
7
4
5
3
LNA
2
DPX
G1
18
SR
1
ST

FIG.1

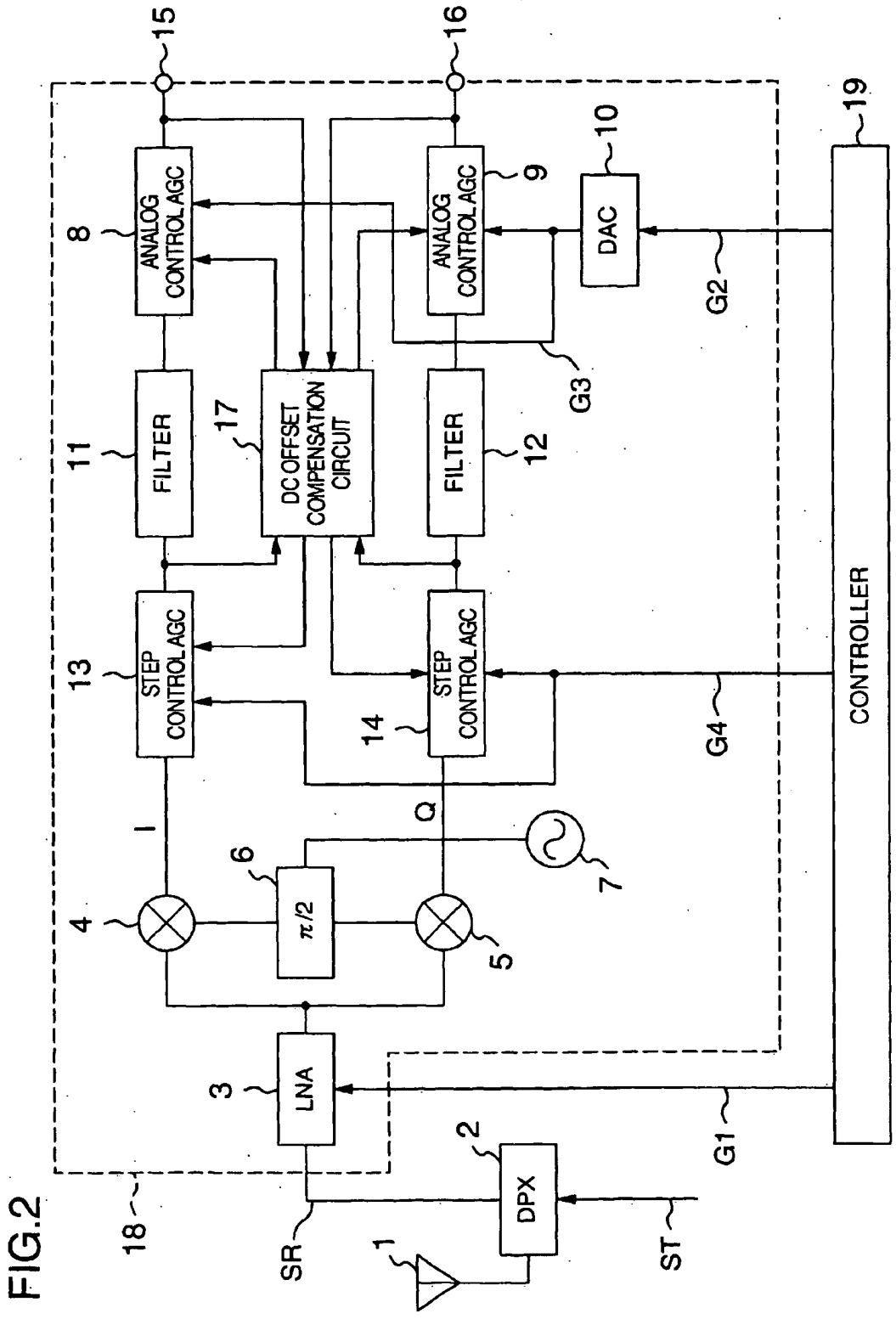

15
16
19
10
8
ANALOG CONTROL AGC
9
ANALOG CONTROL AGC
DAC
G2
G3
11
FILTER
17
DC OFFSET COMPENSATION CIRCUIT
12
FILTER
13
STEP CONTROL AGC
14
STEP CONTROL AGC
G4
CONTROLLER
I
Q
6
π/2
7
4
5
3
LNA
G1
2
DPX
18
SR
1
ST

FIG.2

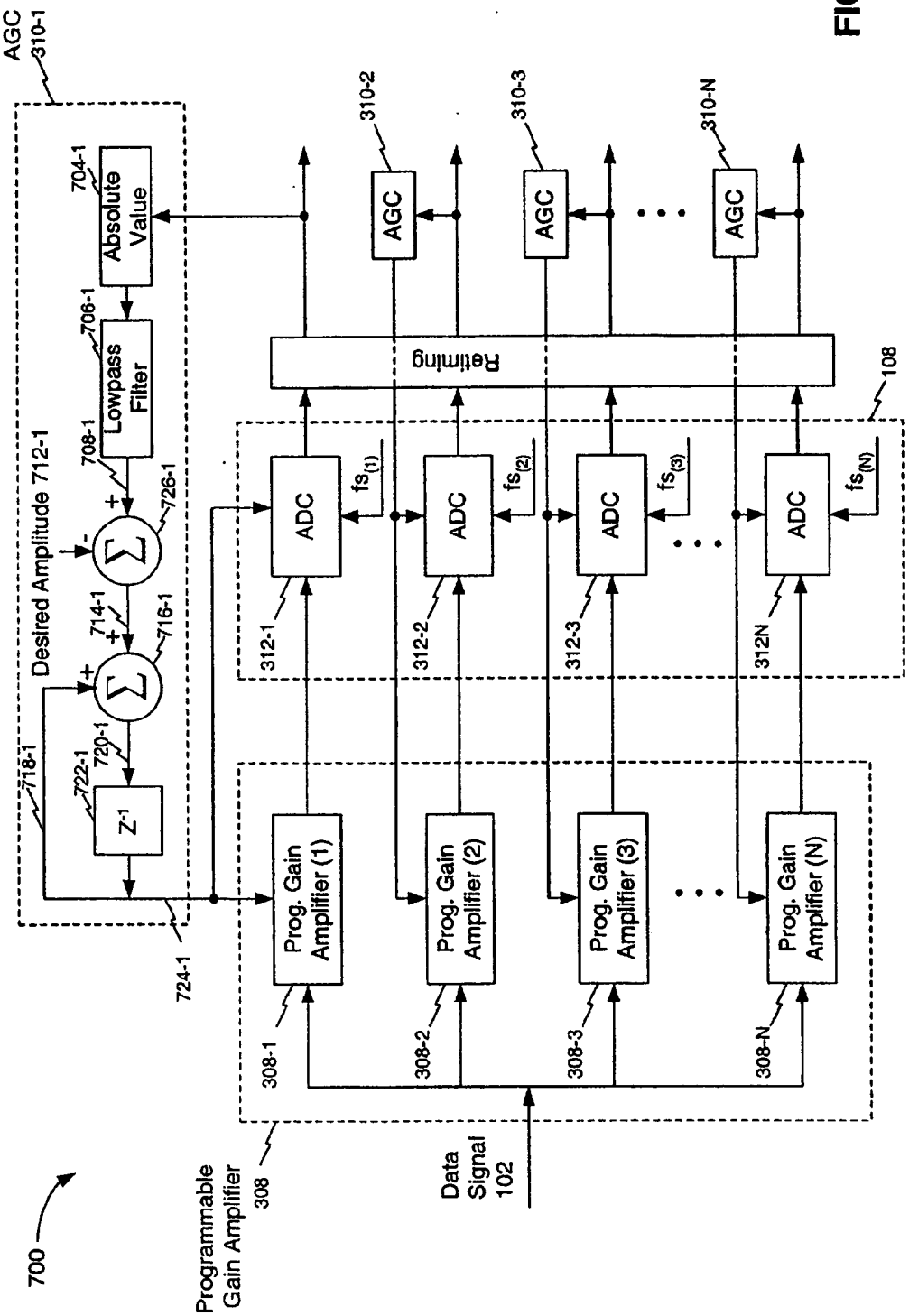

700
Programmable Gain Amplifier
308
Data Signal 102
Prog. Gain Amplifier (1)
Prog. Gain Amplifier (2)
Prog. Gain Amplifier (3)
Prog. Gain Amplifier (N)
308-1
308-2
308-3
308-N
ADC
ADC
ADC
ADC
312-1
312-2
312-3
312N
108
Retiming
AGC
AGC
AGC
AGC
310-1
310-2
310-3
310-N
Absolute Value
Lowpass Filter
Desired Amplitude 712-1
704-1
706-1
708-1
726-1
714-1
716-1
718-1
720-1
722-1
724-1
Z-1

FIG. 7

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Agazzi et al. (43) Pub. Date: Jun. 27, 2002

(54) METHODS AND SYSTEMS FOR DSP-BASED RECEIVERS

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(21) Appl. No.: 10/085,071

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Related U.S. Application Data

(63) Non-provisional of provisional application No. 60/273,215, filed on Mar. 1, 2001. Continuation-in-part of application No. 09/909,896, filed on Jul. 23, 2001, which is a non-provisional of provisional application No. 60/219,918, filed on Jul. 21, 2000.

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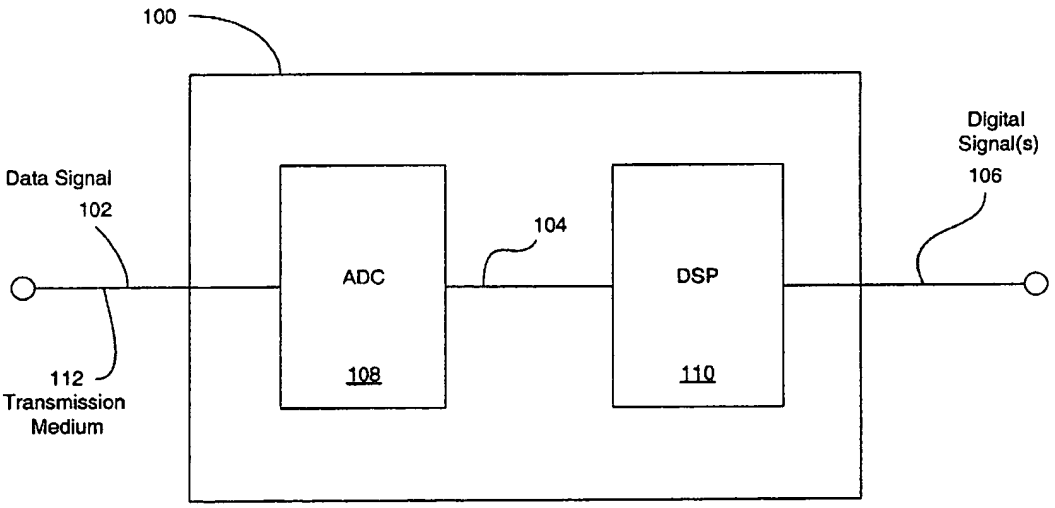
(52) U.S. Cl. 375/355

(57) ABSTRACT

Digital signal processing based methods and systems for receiving data signals include parallel receivers, multi-channel receivers, timing recovery schemes, and, without limitation, equalization schemes. The present invention is implemented as a multi-path parallel receiver in which an analog-to-digital converter ("ADC") and/or a digital signal processor ("DSP") are implemented with parallel paths that operate at lower rates than the received data signal. In an embodiment, a parallel DSP-based receiver in accordance with the invention includes a separate timing recovery loop for each ADC path. The separate timing recovery loops can be used to compensate for timing phase errors in the clock generation circuit that are different for each path. In an embodiment, a parallel DSP-based receiver includes a separate automatic gain control (AGC) loop for each ADC path. The separate AGC loops can be used to compensate for gain errors on a path-by-path basis. In an embodiment, a parallel DSP-based receiver includes a separate offset compensation loop for each ADC path. The separate offset compensation loops can be used to independently compensate for offsets that are different for each path. In an embodiment the present invention is implemented as a multi-channel receiver that receives a plurality of data signals. In an embodiment, one or more of the following types of equalization are performed, alone and/or in various combinations with one another: Viterbi equalization; feed-forward equalization ("FFE"); and/or decision feed-back equalization ("DFE").



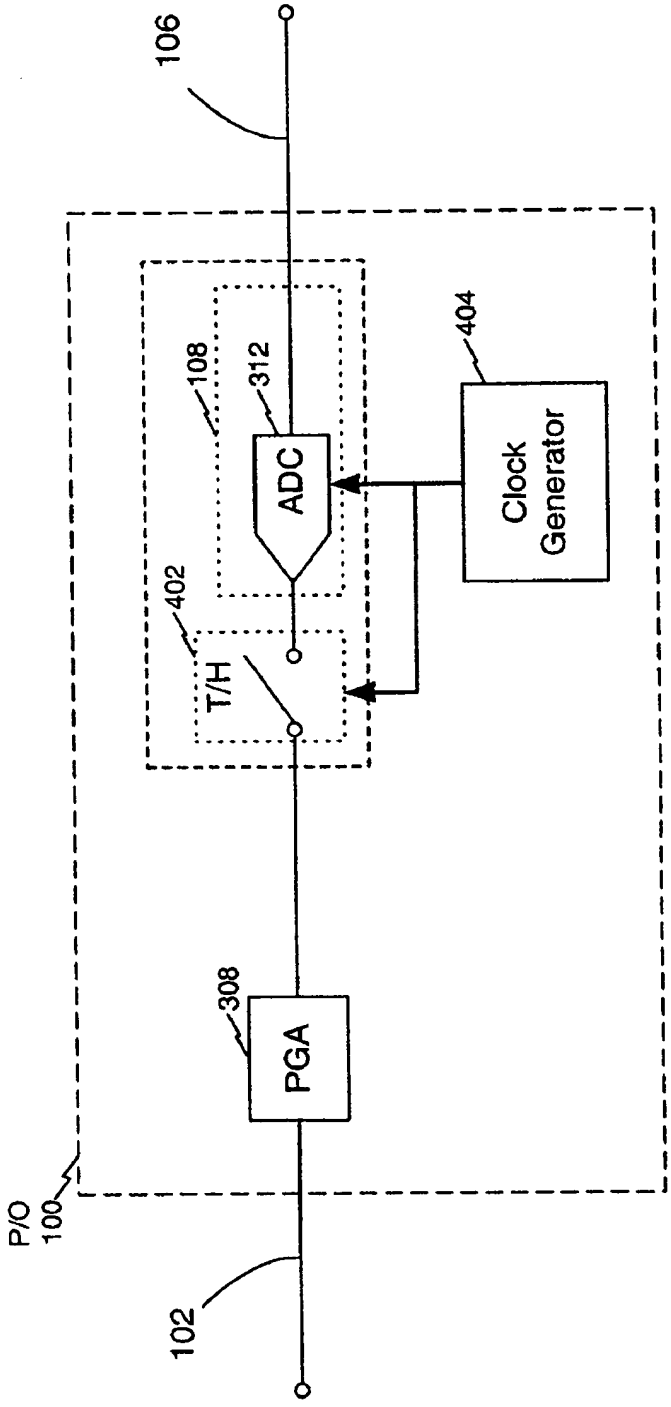


FIG. 4A

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(12) **Patent Application Publication** (10) **Pub. No.: US 2004/0162104 A1**

Ozluturk et al. (43) **Pub. Date: Aug. 19, 2004**

(54) **COMPENSATING FOR ANALOG RADIO COMPONENT IMPAIRMENTS TO RELAX SPECIFICATIONS**

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(73) Assignee: **InterDigital Technology Corporation**, Wilmington, DE

(21) Appl. No.: **10/713,613**

(22) Filed: **Nov. 14, 2003**

Related U.S. Application Data

(60) Provisional application No. 60/427,126, filed on Nov. 15, 2002.

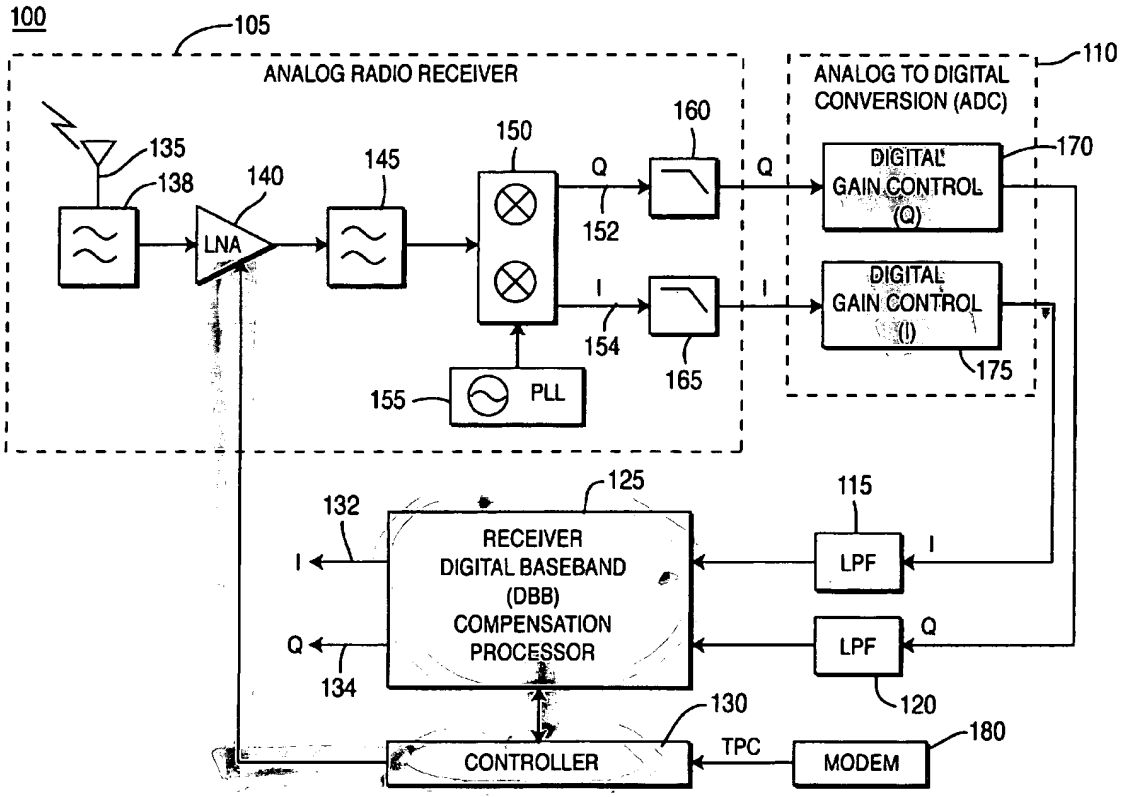
Publication Classification

(51) **Int. Cl.**[7] **H04B 1/40**; H04B 17/00; H04B 1/06; H04B 7/00

(52) **U.S. Cl.** **455/550.1**; 455/84; 455/115.1; 455/127.1; 455/230; 455/232.1; 455/226.1

(57) **ABSTRACT**

In order to compensate for performance degradation caused by inferior low-cost analog radio component tolerances of an analog radio, a future system architecture (FSA) wireless communication transceiver employs numerous digital signal processing (DSP) techniques to compensate for deficiencies of such analog components so that modern specifications may be relaxed. Automatic gain control (AGC) functions are provided in the digital domain, so as to provide enhanced phase and amplitude compensation, as well as many other radio frequency (RF) parameters.



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(12) **United States Patent**
Webster et al.

(10) **Patent No.: US 6,748,200 B1**
(45) **Date of Patent: Jun. 8, 2004**

(54) **AUTOMATIC GAIN CONTROL SYSTEM AND METHOD FOR A ZIF ARCHITECTURE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 4 days.

(21) Appl. No.: **10/407,350**

(22) Filed: **Apr. 4, 2003**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/677,975, filed on Oct. 2, 2000.
(60) Provisional application No. 60/453,905, filed on Mar. 11, 2003.

(51) **Int. Cl.**[7] **H04B 1/06**
(52) **U.S. Cl.** **455/234.1**; 455/232.1; 455/324; 455/296; 455/234.2; 375/345
(58) **Field of Search** 455/232.1, 234.1, 455/234.2, 324, 323, 296, 313, 226.1, 341, 127.1–127.5, 250.1, 78; 375/341, 345

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Assistant Examiner—Lana Le
(74) *Attorney, Agent, or Firm*—Gary R Stanford

(57) **ABSTRACT**

A system and method for controlling amplification of a signal received by a ZIF radio having a power level within a full power range relative to a minimum noise floor. The ZIF radio includes a ZIF receiver front end, an overload detector, an ADC, a saturation detector, a DC and power estimator, and control logic. The control logic utilized full visibility of the ADC to limit gain of the baseband amplifier to a maximum gain setting sufficient to view the minimum noise floor and to view a received signal having a power level within any of several segments of the power spectrum. The segmentation of the power spectrum is based on an overload condition of the ZIF receiver front end and a saturation condition of the ADC. The control logic further employs limited gain stepping of the baseband amplifier to avoid exceeding a DC budget of the ADC.

30 Claims, 9 Drawing Sheets